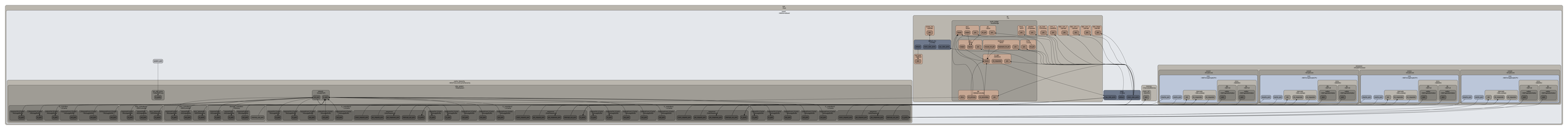

root
: Root
board
: X86DemoBoard
system_port
pc
: Pc
empty_isa
: IsaFake
pio
default_bus
: IOXBar
default
mem_side_ports
cpu_side_ports
bad_addr
: BadAddr
pio
south_bridge
: SouthBridge
pic2
: I8259
inputs
output
pio
pit
: I8254
int_pin
pio
dma1
: I8237
pio
speaker
: PcSpeaker
pio
pic1
: I8259
output
inputs
pio
keyboard
: I8042
mouse_int_pin
keyboard_int_pin
pio
cmos
: Cmos
pio
int_pin
io_apic
: I82094AA
inputs
int_requestor
pio
ide
: X86IdeController
dma
int_primary
int_secondary
pio
pci_host
: PcPciHost
pio
com_1
: Uart8250
pio
fake_com_2
: IsaFake
pio
fake_com_3
: IsaFake
pio
fake_com_4
: IsaFake
pio
fake_floppy
: IsaFake
pio
iobus
: IOXBar
cpu_side_ports
default
mem_side_ports
memory
: ChanneledMemory
mem_ctrl
: MemCtrl
port
processor
: SimpleProcessor
cores3
: SimpleCore
core
: X86TimingSimpleCPU
dcache_port
icache_port
interrupts
: X86LocalApic
pio
int_responder
int_requestor
mmu
: X86MMU
dtb
: X86TLB
walker
: X86PagetableWalker
port
itb
: X86TLB
walker
: X86PagetableWalker
port
cores2
: SimpleCore
core
: X86TimingSimpleCPU
dcache_port
icache_port
interrupts
: X86LocalApic
pio
int_responder
int_requestor
mmu
: X86MMU
dtb
: X86TLB
walker
: X86PagetableWalker
port
itb
: X86TLB
walker
: X86PagetableWalker
port
cores1
: SimpleCore
core
: X86TimingSimpleCPU
dcache_port
icache_port
interrupts
: X86LocalApic
pio
int_responder
int_requestor
mmu
: X86MMU
dtb
: X86TLB
walker
: X86PagetableWalker
port
itb
: X86TLB
walker
: X86PagetableWalker
port
cores0
: SimpleCore
core
: X86TimingSimpleCPU
dcache_port
icache_port
interrupts
: X86LocalApic
pio
int_responder
int_requestor
mmu
: X86MMU
dtb
: X86TLB
walker
: X86PagetableWalker
port
itb
: X86TLB
walker
: X86PagetableWalker
port
cache_hierarchy
: MESITwoLevelCacheHierarchy
ruby_system
: RubySystem
sys_port_proxy
: RubyPortProxy
in_ports
network
: SimplePt2Pt
out_port
in_port
l2_controllers
: L2Cache
responseToL2Cache
: MessageBuffer
in_port
L1RequestToL2Cache
: MessageBuffer
in_port
unblockToL2Cache
: MessageBuffer
in_port
responseFromL2Cache
: MessageBuffer
out_port
L1RequestFromL2Cache
: MessageBuffer
out_port
DirRequestFromL2Cache
: MessageBuffer
out_port
dma_controllers0
: DMAController
responseFromDir
: MessageBuffer
in_port
requestToDir
: MessageBuffer
out_port
dma_sequencer
: DMASequencer
in_ports
dma_controllers1
: DMAController
responseFromDir
: MessageBuffer
in_port
requestToDir
: MessageBuffer
out_port
dma_sequencer
: DMASequencer
in_ports
directory_controllers
: Directory
responseToDir
: MessageBuffer
in_port
requestToDir
: MessageBuffer
in_port
responseFromDir
: MessageBuffer
out_port
memory_out_port
l1_controllers3
: L1Cache
requestToL1Cache
: MessageBuffer
in_port
responseToL1Cache
: MessageBuffer
in_port
requestFromL1Cache
: MessageBuffer
out_port
unblockFromL1Cache
: MessageBuffer
out_port
responseFromL1Cache
: MessageBuffer
out_port
sequencer
: RubySequencer
mem_request_port
pio_request_port
pio_response_port
interrupt_out_port
in_ports
l1_controllers2
: L1Cache
requestToL1Cache
: MessageBuffer
in_port
responseToL1Cache
: MessageBuffer
in_port
requestFromL1Cache
: MessageBuffer
out_port
unblockFromL1Cache
: MessageBuffer
out_port
responseFromL1Cache
: MessageBuffer
out_port
sequencer
: RubySequencer
mem_request_port
pio_request_port
pio_response_port
interrupt_out_port
in_ports
l1_controllers1
: L1Cache
requestToL1Cache
: MessageBuffer
in_port
responseToL1Cache
: MessageBuffer
in_port
requestFromL1Cache
: MessageBuffer
out_port
unblockFromL1Cache
: MessageBuffer
out_port
responseFromL1Cache
: MessageBuffer
out_port
sequencer
: RubySequencer
mem_request_port
pio_request_port
pio_response_port
interrupt_out_port
in_ports
l1_controllers0
: L1Cache
requestToL1Cache
: MessageBuffer
in_port
responseToL1Cache
: MessageBuffer
in_port
requestFromL1Cache
: MessageBuffer
out_port
unblockFromL1Cache
: MessageBuffer
out_port
responseFromL1Cache
: MessageBuffer
out_port
sequencer
: RubySequencer
mem_request_port
pio_request_port
pio_response_port
interrupt_out_port
in_ports